Optimizing Cell-Aware Test Runtime via Functional Fault Correlations

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Abstract

As integrated circuits scale, traditional fault models are often insufficient for detecting intra-cell defects, necessitating the adoption of Cell-Aware Test (CAT) to ensure high test quality and reduce defective parts per million (DPPM). However, the deployment of CAT is hindered by significant computational overheads during both the library characterization and fault simulation phases. This research addresses these efficiency challenges by systematically exploiting the correlations and equivalencies between physical intra-cell defects and traditional functional fault models (e.g., Stuck-At, Transition Delay, and Small-Delay Defects).

The work first evaluates the effectiveness of functional testing paradigms, specifically Software-Based Self-Test (SBST), demonstrating that test programs targeting stuck-at faults can achieve high diagnostic coverage (up to 87%) for static CAT faults on RISC-V cores without specific CAT targeting. Building on this correlation, the research introduces the FACT (Fault Analysis for Cell-aware Test) methodology, which optimizes the fault simulation phase. By prioritizing faster-to-simulate traditional fault models that correlate with CAT defects, simulation runtimes are reduced by up to 80% for static and 35% for dynamic faults. Finally, to address the bottleneck of library characterization, the EquivalentID methodology is proposed. This pre-processing framework applies structural and propagation rules to identify transistor-level defects equivalent to functional faults, removing them from the SPICE simulation queue and reducing characterization runtime by approximately 7.3% while preserving diagnostic resolution.